IN THE SPECIFICATION:

Please replace paragraph number **[0004]** with the following rewritten paragraph:

[0004] Following fabrication of a plurality of dice on a wafer or other bulk substrate of semiconductor material, a cursory test for functionality is conducted on each die, such as by probe testing. The dice are then singulated, and those passing the functionality test are picked from the wafer, typically for packaging, such as by transfer molding, and subsequent incorporation into a higher-level assembly. Typically, each die is formed with one or more rows of bond pads on the active surface. The bond pad row or rows may be formed along a central axis of the die or along one or more peripheral portions thereof. Transfer molded packages may comprise bond wires which electrically couple bond pads on the die to leads of a lead frame, the outer ends of the leads extending beyond the protective encapsulant, which is typically a ~~silicon~~ silicone-filled, thermoplastic polymer. The lead frame leads are used to achieve mechanical and electric connection of the die to a carrier substrate such as a printed circuit board (PCB), for example.

Please replace paragraph number **[0007]** with the following rewritten paragraph:

[0007] A board-on-chip (BOC) semiconductor package has also been developed, in which an interposer substrate such as a relatively small, slightly larger than die-size interposer substrate is formed with a centrally placed, elongate through-slot sized and configured for alignment with a row or rows of bond pads on the die. The through-slot is also known as an "interconnect slot" or "wire bond slot". The die is adhesively joined by its active surface to one side of the interposer substrate such that the bond pads are accessible through the interconnect slot. The bond pads are connected to conductive traces on the opposite side of the interposer substrate, by bond wires, for example, which pass through the interconnect slot. The interconnect slot is then filled with a filled polymer encapsulant to encase and seal the bond wires and surrounding, exposed portion of the die's active surface. Conventionally, a transfer molding process is used to form this wire bond mold cap while simultaneously encapsulating the

backside and sides of the die on the opposite side of the interposer substrate. A ball grid array (BGA) or other type of array of discrete conductive elements electrically connected to the conductive traces and projecting from the side of the interposer substrate with the wire bond cap may be used to mechanically and electrically connect the package to a carrier substrate or other higher-level packaging. Various examples of this type of package construction are shown in U.S. Patent Nos. 5,723,907 and 5,739,585 to Akram and 5,818,698 to Corisis, all of which patents are assigned to the assignee of the present application and the disclosure of each of which is incorporated by reference herein. The resulting package has a much reduced size, which may be termed "chip scale" or "near chip scale," and is generally capable of establishing robust, ~~high-~~ high-quality mechanical and electrical connections using conventional bonding techniques.